SPECIFICATION

Electronic Version 1.2.8

Stylesheet Version 1.0

An optimum UMTS Modem for multimedia Data, Voice, VoIP in wireless Internet applications.

Cross Reference to Related Applications

Referenced-applications

This patent is based on the development of IP core product for 3G wireless mobile communications by IComm Technologies, Inc. This patent is related to U.S. patent application number 09/681093 entitle "Turbo Codes Decoder".

Background of Invention

Field of the Invention

[0001] This invention relates to UMTS Modem for 3G Wireless Mobile Communications; and more particularly, to a very high speed UMTS Modem using Turbo Codes Encoder/Decoder and channels hopping with Orthogonal Frequency Division Multiplexing method implemented by complex FFT/iFFT processors for multimedia Data, Voice, VoIP in wireless Internet applications.

Description of the Prior Art

[0002] UMTS stands for Universal Mobile Telecommunications System. UMTS is a part of the IMT-2000, a global family of 3G mobile communications systems delivering high-value broadband information, commerce and multimedia entertainment services to mobile users via fixed, wireless and satellite IP networks. Modem stands for modulation and demodulations. When a base station sending digital information to the terminal handset, the modem at the base station converts the digital data into analog signal and transmits it over the air, and the terminal

handset modem receives the signal and converts the analog signal back into digital data. As shown in FIGURE 1. digital data from the MAC layer 15 is shifted into the UMTS modem transmitter where data is encoded for error-correction, then modulated and sent to the analog front-end 16 for transmitting over the air. Received signal from the analog front-end 16 enters the UMTS modem receiver 13 where it is demodulated by a baseband processor, then shifted to the MAC layer 15. The Turbo Codes baseband processor is used to encode data and to reconstruct the corrupted and noisy received data and to improve BER data throughput in a limited power and noisy environment. The Orthogonal Frequency Division Multiplexing is a technique to divide the broadband channel into sub-channels where multiple adjacent channels transmit their carriers' frequency which are orthogonal to each other, the sum of all carriers can be transmitted over the air to the receiver where each channel's carrier can be separated without loss of information due to interferences. FIGURE 2. shows an example of an 8-PSK constellations where each group of 3-bit data is mapped in to a point with an in-phase (I) and quadrature (Q) coordinates.

Summary of Invention

[0003] The present invention provides improved methods and architecture of an UMTS modem for delivering optimum high-speed broadband information, commerce and multimedia entertainment services to mobile users via fixed, wireless and satellite IP networks. The present invention utilizes Turbo Codes baseband processor for optimum performance in decoding received data in limited power and noisy environments. The invention presents a method to divide the UMTS broadband into multiple sub-channels and the uses of an Orthogonal Frequency Division Multiplexing method implemented by N-point complex FFT/iFFT processors in which it effectively divides the broadband high-speed channel into multiple slow-speed N sub-channels where multiple adjacent channels transmit their carriers' frequency which are orthogonal to each other. The high-speed bit-stream is also sub-divided into multiple slow-speed sub bit-streams. An example, the total broadband channel capacity is R-Mbps, then the slower sub-channel capacity S-Mbps is equal to (R-Mbps)/N. Therefore, it is most advantageous for the Turbo

Codes baseband processor since it performs much better in slower bit rate with more number of iterations. The present invention utilizes an M-bit serial-to-parallel (S/P) converter to sub-divides the input high-speed R-Mbps bit-stream into multiple M slow-speed S-Mbps bit-streams where each bit-stream will be transmitted in the assigned channel. Each bit-stream is encoded one bit per cycle with the Turbo Codes encoder and then mapped into an 8-PSK constellation point where its I and Q components are mapped into the real and imaginary part of the a complex iFFT point. Since M is less than or equal to N, channel hopping can be done by assigning a bit-stream to a new channel once its current channel getting noisy. Accordingly, several objects and advantages of the present invention are:

[0004] To deliver high-quality, high-speed broadband information to wireless IP network.

[0005] To utilize Turbo Codes baseband processor, rate 1/3, 8-state SISO Log-MAP, for optimum performance in decoding received data.

[0006] To utilize an M-bit serial-to-parallel (S/P) converter to sub-divide the input high-speed bit-stream into multiple M slow-speed bit-stream.

[0007] To utilize an Orthogonal Frequency Division Multiplexing method implemented by N-point complex FFT/iFFT processor to sub-divide the broadband high-speed channel into multiple slow-speed N sub-channels.

[0008] To implement channel hopping to re-assign new channel once the old channel getting noisy.

[0009] To utilize guard-interval (GI) addition to minimize intersymbol interferences.

[0010] Still further objectives and advantages will become apparent to one skill in the art from a consideration of the ensuing examples, descriptions and accompanying drawings.

Brief Description of Drawings

[0011] FIGURE 1. An UMTS Modem System Block Diagram (Prior Art).

[0012] FIGURE 2. An 8-PSK Constellations (Prior Art).

[0013] FIGURE 3. An UMTS Modem Transmitter Functional Block Diagram.

[0014] FIGURE 4. An UMTS Modem Receiver Functional Block Diagram.

Detailed Description

[0015] As shown in FIGURE 1. an UMTS modem 11 comprises of an modem transmitter 12 for modulating digital data and sending signal over the air, a modem receiver 13 for demodulating received signal and converting it into digital data, and an AFC Clock Recovery circuitry for recovering clock and synchronization..

UMTS Modem Transmitter

[0016] As shown in FIGURE 3. an UMTS modem transmitter 12 comprises of an M-bit serial-to-parallel (S/P) converter31 to convert input bit-stream into an M number of sub bit-streams, an M number of Turbo Codes encoder 32 with coding rate 1/3 and constraint length K=4 corresponding to each bit-stream, an M number of Mapper 33 for 8-PSK modulation corresponding to each channel, a Channel Selector for assigning each bit-stream to a sub-channel, an N-point complex iFFT processor 34 for implementing multiple sub-channels with Orthogonal Frequency Division Multiplexing method, a guard interval (GI) adder 35 for adding guard interval, a Symbol Wave Shaper 36, and an IQ Modulator 37 for modulation the transmit signal with a carrier, a Carrier generator 38 produces carrier frequency.

[0017] As shown in FIGURE 3. and FIGURE 1., the UMTS modem transmitter 12 functions effectively as follows:

[0018] High-speed R-Mbps input serial data is shifted into the M-bit serial-to-parallel (S/P) converter 31 to generate the slow-speed S-Mbps M serial sub bit-streams (labeled from 0 to M-1).

[0019] Each sub bit-stream is shifted serially into its own Turbo Codes encoder 32, with coding rate 1/3 and constraint length K=4, one bit per cycle where it is converted into a 3-bit symbol output (one data bit and two parity bits).

[0020] The 3-bit symbol 22 is shifted into the 8-PSK Mapper33 where it is mapped into a constellation point 21 as shown in FIGURE 2. The values of its I and Q components are selected from the Table 1. The output of the 8-PSK Mapper 33 is a set of (I,Q) values corresponds to the Real and Imaginary parts of a point in the complex iFFT processor.

[0021] The (I,Q) values are shifted into the Channel Selector 39 where each set of (I,Q) is assigned to a point in the N-point complex iFFT processor. When channel hopping is required, the Channel Selector 39 can re-assign a new point for that requested set of (I,Q).

[0022] The complex iFFT Processor 34 perform the invert complex fast Fourier transform (iFFT) to produce N complex samples which are then separated into an I sequence and a Q sequence of N samples correspond the real and imaginary parts.

[0023] The I and Q sequences are shifted completely through the GI Adder 35 where the guard interval is added to each I and Q sequences.

[0024] The I and Q sequences are then shifted completely through the Symbol Wave Shaper 36 where the I and Q sequences are modified by a symbol wave-shaper FIR filter.

[0025] The I and Q sequences are then shifted completely through the IQ Modulator 37 where the I sequence is modulated with Sine carrier 38, and the Q sequence is modulated with a Cosine carrier 38. The summation of the modulated I and Q sequences produces the transmit signal output.

UMTS Modem Receiver

[0026]

As shown in FIGURE 4. an UMTS modem receiver 13 comprises of an IQ demodulator 41 for demodulating the receive signal with a carrier, a local carrier generator 48 produces carrier frequency, an AFC Clock circuitry 47, a guard interval (GI) remover 42 for deleting guard interval, an N-point complex FFT processor 43 for implementing multiple sub-channels with Orthogonal Frequency Division Multiplexing method, an M number of de-Mapper 44 for 8-PSK

demodulation corresponding to each channel, an M number of Turbo Codes Decoder baseband processor 45 with coding rate 1/3 and constraint length K=4 corresponding to each bit-stream, an M-bit parallel-to-serial (P/S) converter 46 to convert the M input sub bit-streams into a final bit-streams output.

[0027] As shown in FIGURE 4. and FIGURE 1., the UMTS modem receiver 13 functions effectively as follows:

[0028] Receive signal entering the IQ Demodulator 41 is demodulated with a local carrier 48 to produce the I and Q sequences of N samples.

[0029] The I and Q sequences are shifted completely through the GI Remover 42 where the guard interval is remove from each I and Q sequence.

[0030] The I and Q sequences are then shifted completely into the N-point complex FFT Processor 43. The FFT Processor 43 performs complex Fast Fourier Transform (FFT) for the I and Q sequences of N samples to convert them into N complex points data.

[0031] The Channel De-selector 49 then selects each complex point data for each set of (I,Q) values correspond to each of the M bit-streams.

[0032] Each set of (I,Q) is shifted into the 8-PSK De-Mapper 44 where it is convert into a soft-decision value output.

[0033] The soft-decision value data is shifted into the Turbo Codes Decoder baseband processor 45, where data is iteratively decoded until a final dicision hard-decoded bit is produced for the output correspond to each bit-stream.

[0034] The hard-decoded output bit is latched into the M-bit parallel-to-serial (P/S) 46, where the all the M-bit data is serially shifted to the output.